CLAIMS

What is claimed is:

1. A circuit comprising:

a first phase-locked loop (PLL) to receive a first reference signal and a first feedback signal, and to produce a data clock signal having a first frequency based at least in part upon differences between the first reference signal and a first feedback signal; and

a second PLL coupled to the first PLL to receive a second reference signal and a second feedback signal, and to produce a second clock signal having a second frequency based at least in part upon differences between the second reference signal and the second feedback signal, the first feedback signal and the second reference signal being derived from the data clock signal and the second feedback signal being derived from the second clock signal.

2. The circuit of claim 1, further comprising a first divide-by-N circuit coupled to the first PLL circuit to divide the first frequency of the data clock signal by a first integer value N to produce the first feedback signal having a third frequency.

3. The circuit of claim 2, further comprising a divide-by-M circuit coupled between the first PLL circuit and the second PLL circuit to divide the first frequency of the data clock signal by an integer value M to produce the second reference signal.

4. The circuit of claim 3, wherein the divide-by-M circuit is equipped to divide the first frequency of the data clock signal by a selected one of a factor of 4, 2 and 1.

5. The circuit of claim 4, wherein the first divide-by-N circuit comprises a divide-by-4 circuit to divide the first frequency of the data clock signal by a factor of 4.

6. The circuit of claim 3, further comprising a second divide-by-N circuit coupled to the second PLL to divide the second frequency of the second clock signal by a second integer value N to produce the second feedback signal, wherein the second integer value N is selected from a group of integer values including a low integer value, and a high integer value that is less than two times the low integer value.

7. The circuit of claim 1, wherein a bandwidth of the second PLL is at least three times greater than a bandwidth of the first PLL.

8. The circuit of claim 1, further comprising:

a first signal path corresponding to the second reference signal; and

a second signal path corresponding to the second feedback signal, wherein the first and second signal paths are equivalent in length.

9. A microprocessor comprising:

a processor core;

I/O circuitry; and

a clock generation circuit comprising:

a first phase-locked loop (PLL) circuit to produce a first output signal having a first frequency based at least in part upon a first reference signal and a first feedback signal derived from the first output signal, the first output signal to be used as a data clock signal for the I/O circuitry; and

a second PLL circuit coupled to the first PLL to produce a second output signal having a second frequency based at least in part upon a second reference signal derived from the first output signal and a second feedback signal derived from the second output signal, the second output signal to be used as a clock signal for the processor core.

10. The microprocessor of claim 9, further comprising a first divide-by-N circuit coupled to the first PLL circuit to divide the first frequency of the data clock signal by a first integer value N to produce the first feedback signal having a third frequency.

11. The microprocessor of claim 10, further comprising a divide-by-M circuit coupled between the first PLL circuit and the second PLL circuit to divide the first frequency of the data clock signal by an integer value M to produce the second reference signal.

12. The circuit of claim 11, wherein the divide-by-M circuit is equipped to divide the first frequency of the data clock signal by a selected one of a factor of 4, 2 and 1.

13. The circuit of claim 12, wherein the first divide-by-N circuit comprises a divide-by-4 circuit to divide the first frequency of the data clock signal by a factor of 4.

14. The circuit of claim 11, further comprising a second divide-by-N circuit coupled to the second PLL to divide the second frequency of the core clock signal by a second integer value N to produce the second feedback signal, wherein the second integer value N is selected from a group of integer values including a low integer value and a high integer value that is less than two times the low integer value.

15. The circuit of claim 9, wherein a bandwidth of the second PLL is at least three times greater than a bandwidth of the first PLL.

16. The circuit of claim 9, further comprising:

a first signal path corresponding to the second reference signal; and

a second signal path corresponding to the second feedback signal, wherein the first and second signal paths are equivalent in length.

17. In a microprocessor, a method comprising:

disposing a first of at least two phase locked loops in a cascaded arrangement, such that the first PLL produces a first output signal suitable for use as a data clock having a first frequency based at least in part upon a first reference signal and a first feedback signal derived from the data clock signal; and

disposing a second PLL in communication with the first PLL, such that the second PLL produces a second output signal suitable for use as a core clock having a second frequency based at least in part upon a second reference signal derived from the first output signal and a second feedback signal derived from the second output signal.

18. The method of claim 17, wherein the first reference signal comprises an external bus clock signal having a third frequency.

19. The method of claim 17, further comprising:

dividing the data clock signal by a first integer value to attain the first feedback signal;

dividing the data clock signal by a second integer value to attain the second input signal; and

dividing the second output signal by a third integer value to attain the second feedback signal.